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Performance Analysis Ofmulti Channel Adc Using Mts Algorithm

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Abstract- *The Proposed system uses a multi-channel low power Digital rampanalog-to-digital converter (ADC). A Metastable-then-set (MTS) algorithm is proposed to eliminate the Metastabilty problem and its effects on power consumption and performance also have been measured. A prototype ADC was implemented in 0.13-nm CMOS technology and operated under a 1.2 V supply. At a sampling rate of 20 MS/s.The measured total power dissipation of a single channel ADC is 475 μW. The proposed flag synchronization technique minimizes the crosstalk among the channel.The VLSI implementation was done using Xilinx and Multisim Simulator.*

KeyWords: Digital Ramp ADC, low Power, Multi channel, Metastable-then-set (MTS)

I INTRODUCTION

As advanced CMOS technologies enhance the operational speed of microelectronics, successive approximation register (SAR) analog-todigital converters (ADCs) have recently become a very popular ADC architecture, having a low power characteristic and utilizing new design techniques [1]–[7]. With this trend, recently reported SAR ADCs cover a wide range of performances (see Fig. 1) from low frequencyapplications such as wireless sensor networks (Group A) [5] to gigahertz applications including optical communications (Group C) [4].Most ADC applications today can be divided into four broad market segments: Data Acquisition, Precision Industrial Measurement, Voiceband and Audio, and High Speed ("High Speed" implying sampling rates greater than approximately 10MSPS—although this line of demarcation is somewhat arbitrary. For instance, a 2MSPS sampling rate certainly qualifies as "high speed" for an 18-bit SAR ADC). A very large percentage of these applications can be filled with either the Successive Approximation (SAR), Sigma-Delta (Σ-Δ), or Pipelined ADC. A basic understanding of the three most popular ADC architectures is therefore valuable in selecting the proper ADC for a given application.

A. Basics Of SARADC

Comparing to other SARADCit seems allowing the lowest-power consumption. This architecture has the advantage to be very simple; it implements the binary search algorithm. Power dissipation scales with the sample rate, unlike flash ADCs that usually have constant power dissipation versus sample rate. This is especially useful in low-power applications. Moreover SAR ADC does not contain an operational amplifier; that are generally power-hungry, it needs just one comparator that consume much less power than operational amplifiers.

SAR ADC has four mains building blocks(Figure 1.1):

- Sample-and-Hold Stage (S/H)
- Digital-to-Analog Converter (DAC)

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- Comparator
- Successive Approximation Register (SAR)

The basic functionality of a SAR ADC is very simple (Figure 1.1). The analog input voltage V_{IN} is sampled by the Track & Hold block. To implement the binary search algorithm, the N-bit register is first set to mid scale setting the MSB to '1' and all other bits to '0'. This forces the DAC output, V_{DAC}, to be half of the reference voltage, $V_{REF}/2$. V_{IN} is then compared with V_{DAC}, if V_{IN} is greater than V_{DAC}, the comparator output is logic 1 and the MSB of the N-bit register remains at 1. The basic functionality of a SAR ADC is very simple (Figure 1.1). The analog input voltage V_{IN} is sampled by the Track & Hold block. To implement the binary search algorithm, the N-bit register is first set to mid scale setting the MSB to '1' and all other bits to '0'. Conversely, if V_{IN} is less than V_{DAC} the comparator output is logic 0 and the MSB of the register is cleared to 0. The SAR control logic then moves to the next bit down, forces that bit high, and does another comparison. The sequence continues all the way down to the LSB. Once this is done, the conversion is completed, and the N-bit digital word is available in the register.bits to '0'. This forces the DAC output, V_{DAC}, to be half of the reference voltage, $V_{REF}/2$. V_{IN} is then compared with V_{DAC}.

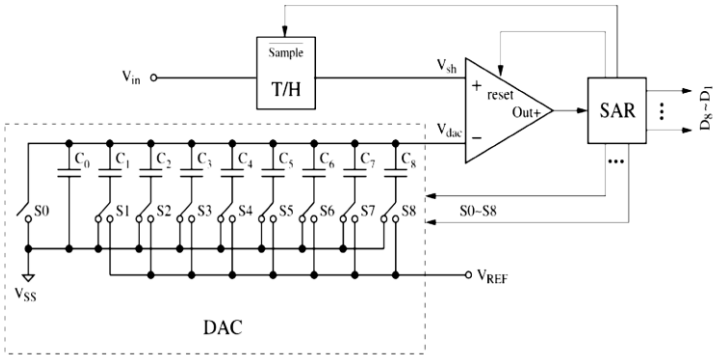

Figure 1.1Simplified N-bit SAR ADC architecture

B. Theory OfMetastability

Metastability is a problem that occurs inall latching comparators when the input is near the comparator decision point.The problem occurs when the comparator takes more time to switch to a valid output state than is available in the sample interval.Otherwise Metastability in digital systems occurs when two asynchronous signals combine in such a way that their resulting output goes to an indeterminate state.

II BLOCK DIAGRAM

A.MTS Algorithm

The self-triggering operation of ASAR ADCs removes the need for a high speedinternal clock and speeds up the total conversion . However, when the input to the comparator is very small, the latching operation suffers from metastability and conversion takes an unusuallylong time. Figure 2.1 (a) depicts a simple block diagram of a typical ASAR ADC with several important waveforms [Figure 2.1(b)]. Except for the first latching command , all the following latching operations are self-conducted by sensing the comparator output with an XOR function. The XOR sets the signal to notify the bit-decision completion when the output is regenerated. The time for the following operations such as digital-to-analog converter (DAC) settling is then defined by with fixed pulse width (flag Ext).After the MSB decision is completed, the MSB-1 bit decision takes place and it takes much longer time than others decisions due to theMetastability(VDAC≈VSH).The remaining LSBs are sequentially decided to be zeros by following the conventional SAR algorithm. In order to guarantee that the conversion is finished in a given time, the metastability problem must be resolved. Unlike other designs that try to conduct all the decision cycles or assign unresolved codes after conversion , the proposed metastable-then-set (MTS) algorithm sets unresolved codes on chip and completes the conversion when metastability is detected. By doing this, the MTS algorithm prevents the metastability from reducing the conversionspeed and eliminates unnecessary decision cycles. Figure 2.2 shows the modified block diagram of the ASAR ADC with a metastability detector (MD) for implementation of the MTS algorithm [see Figure 2.2(a)] and its waveforms [see Figure 2.2(b)]. Tmeta from the ASAR logic rises.

B. MTSImplementation

In order to validate the MTS algorithm at a prototype level, an MD block was designed with the operational principlewith the operational principle shown in Fig.2.3.Tmeta with a constant pulse width of tMTS is replaced by a ramp signal (ramp) for test

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purposes. The ramp signal rises with latch if the ramp reaches a decision threshold (VTH_meta) before the latching is complete (falling of latch signal), i.e., before the flag appears, then the situation is considered to be metastable and the meta signal turns on. Thus, the time when VTH_meta meets is defined as tMTS. The ramp signal is reset when the flag (in normal conversion) or meta (in metastable status) appears. tMTS is a key variable to control .and it is adjusted externally by changing the slope of the ramp . By increasing the slope of the ramp under a fixed VTHreduces and α increases.

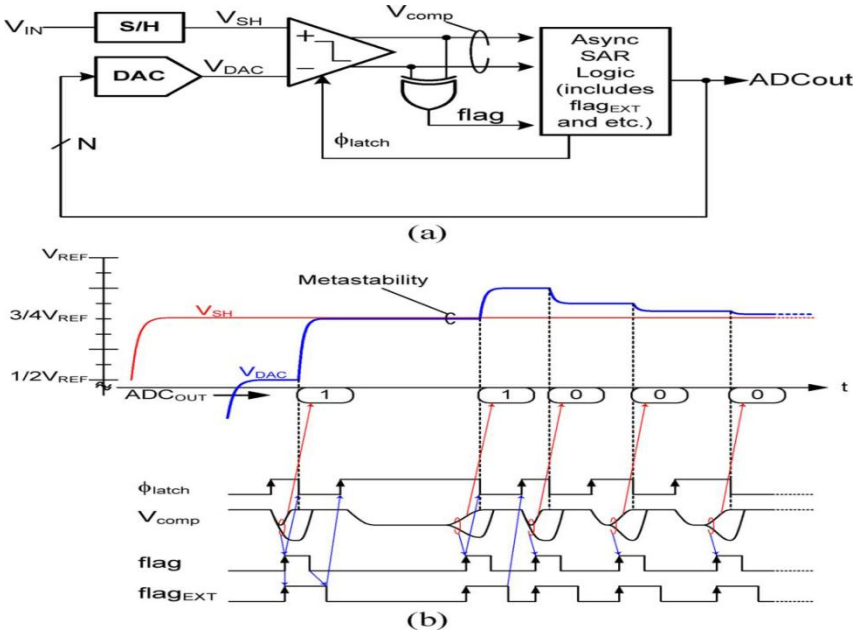

Figure 2.4(a)showsthe hardware implementation of the MD explained above. The ramp generator has a simple integrator composed of a current source (I MD) and a capacitor (C MD). At the rising edge of , the integrator begins to charge CMD. Integration finishes either when flag =1 (decision completion) or when metastabilityis detected (when node *A* reaches the logic threshold of the following inverter,inv 1 Here, the logic threshold of inv 1 plays the role of VTH_meta in Fig 2.3. and the value is approximately half the supply voltage. When metastability is detected, a latch composed of inv1 and inv2 holds the meta =1 until the next input is sampled. The amount of IMD is controlled externally to control the slope of the ramp. Figure 2.4 (b) shows the simulation waveforms of the MD in Figure 2.4 (a) for two cases: (upper waveform) without and (lower waveform) with metastability occurrence.

C. Drawbacks of Existing Method

1) Require N iterations required
2) DAC settling and accuracy limitperformance
3) Only two channels are implemented
4) Processing time is high due to more hardware complexity
5)Sampling rate is less

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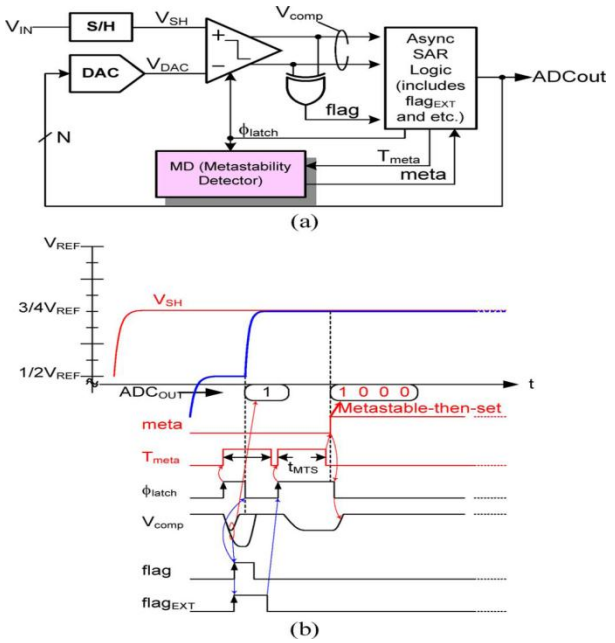

Figure 2.2 (a) Modified asynchronous SAR ADC for the MTS algorithm and (b)its timing diagram

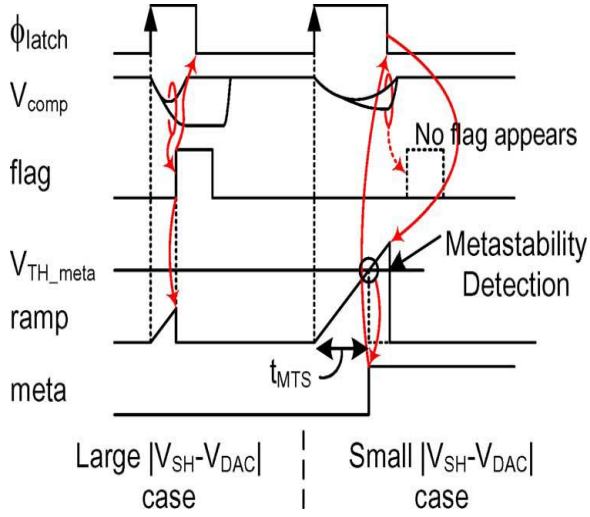

Figure 2.3 MTS implementation-based Rampgeneration for testability

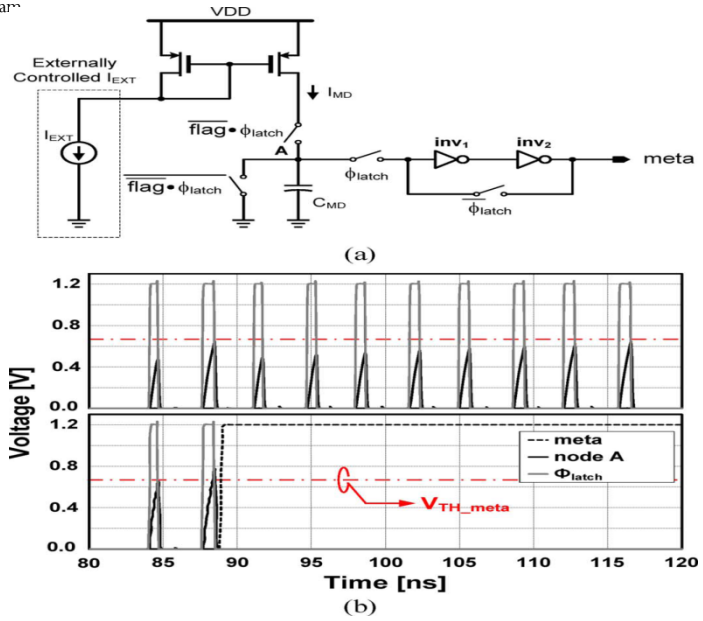

Figure 2.4(a) Hardware implementation of metastabledetector and (b) its simulation result:

III. PROPOSEDMODEL

A.Operationof Digital Ramp ADC

Figure 3.1 Also known as the stair step -ramp, or simply counter A/D converter, this is also fairly easy to understand but it is unfortunately suffers from several limitations. The basic idea is to connect the output of a free-running binary counter to the input of a DAC, then compare the analog output of the DAC with the analog input signal to be digitized and use the comparator's output to tell the counter when to stop counting and reset. The following schematicshows the basic idea: As the counter counts up with each clock pulse, the DAC outputs a slightly higher (more positive) voltage. This voltage is compared against the input voltage by the comparator. If the input voltage is greater than the

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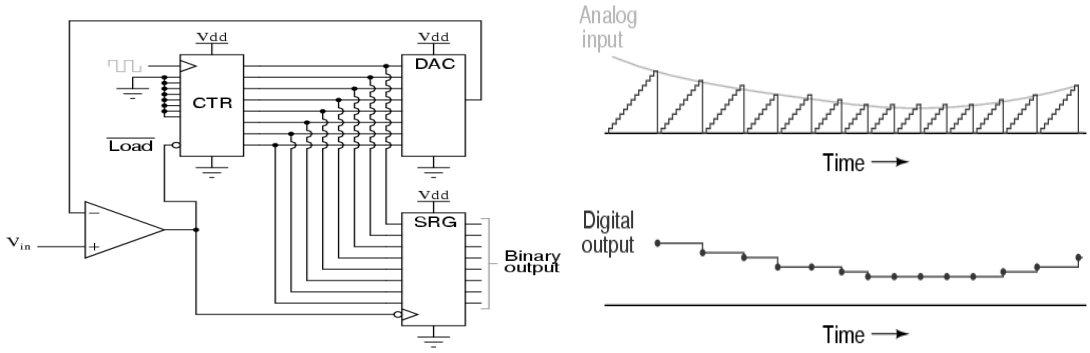


Figure 3.1 Digital Ramp ADCFigure 3.2 Digital Ramp ADC wave form

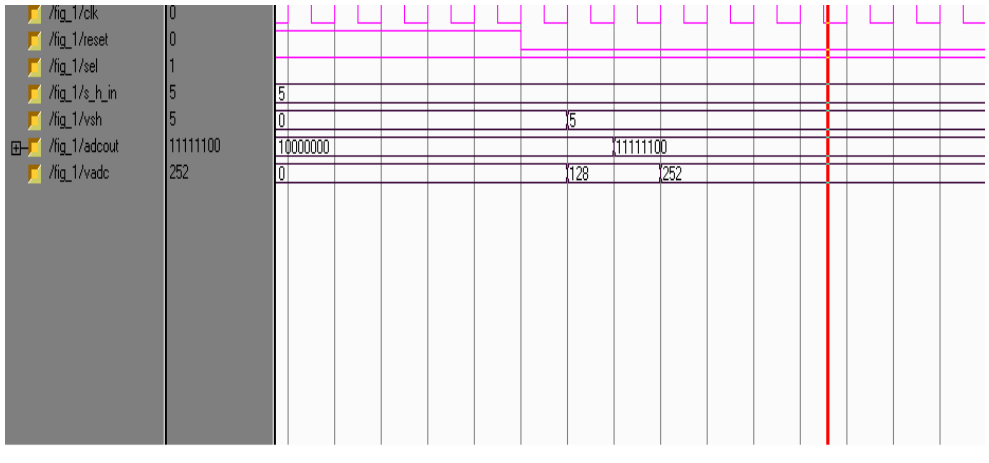
DAC output, the comparator's output will be high and the counter will continue counting normally. Eventually, though, the DAC output will exceed the input voltage, causing the comparator's output to go low. This will cause two things to happen: first, the high-to-low transition of the comparator's output will cause the shift register to "load" whatever binary count is being output by the counter, thus updating the ADC circuit's output; secondly, the counter will receive a low signal on the active-low LOAD input, causing it to reset to 00000000 on the next clock pulse. From the figure (3.2)The effect of this circuit is to produce a DAC output that ramps up to whatever level the analog input signal is at, output the binary number corresponding to that level, and start over again.

B. Methodology Used

A Metastable-then-set (MTS) algorithm is proposed to eliminate the Metastability problem in the multi-channel Digital ramp type analog-to-digital converter (ADC). and its effects on power consumption and performance also have been measured. The flag synchronization technique minimizes the crosstalk among the channels.A prototype ADC was implemented in 0.13-nm CMOS technology and operated under a 1.2 V supply. At a sampling rate of 20 MS/s. The measured total power dissipation of a single channel ADC is 475 µW.

IV RESULT AND PARAMETERSMEASUREMENT

A.Simulation Results



Fiure 4.1 Logical Output Waveform for asynchronous SARADC

WITH METASTABILITY WITHOUT METASTABILITY

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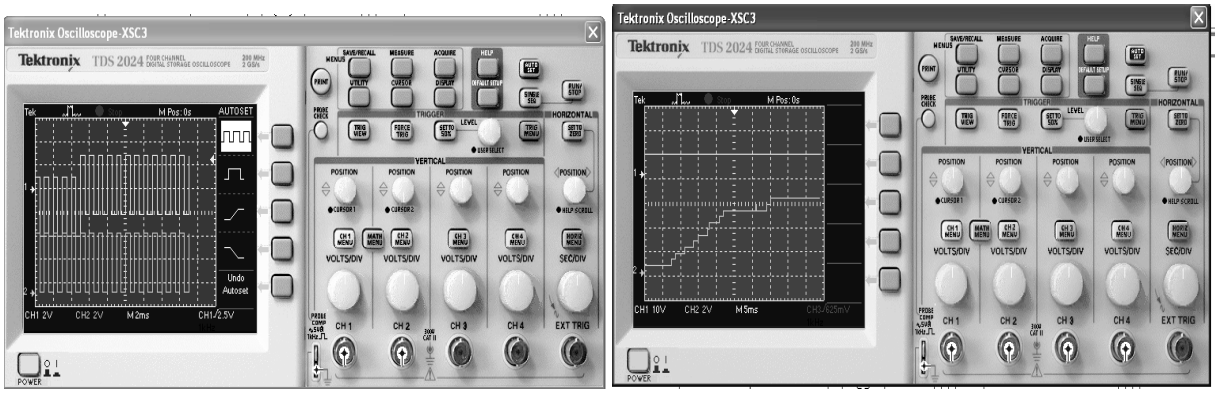

B. Parameters Measured

The proposed VLSI architecture of Digital Ramp ADC was implemented using VHDL.

TABLE I :Parameters Value

Process	CMOS 0.13 µm	
Active Area	500 x 1550 µm2	
Sampling Rate	17.5 MS/ s	
Power consumption (Single channel)	Analog	66 µW @ 1.2 V
	Digital	372 µW @ 1.2 V
	DAC Switching	132 µW @ 1.2 V
	Total	570 µW @ 1.2 V
Effective number of bits	8.3 bits	

V CONCLUSION

This paper investigates the potential usage of an ASAR ADC for a dual-channel ADC with solutions for metastability and crosstalk. The MTS algorithm not only solves the metastability problem but also showspossible power savings. The flag synchronization technique reduces the crosstalk between two channels and makes it possible to share a common reference for better dynamic performance.

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